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PATENT APPLICATION
ATTORNEY DOCKET NO. LMRX-P029/P1180

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: CHENG et al.	Examiner: Everhart, Caridad
Application No. 10/738,360	Group No.: 2829
Filed: 12-16-2003	Confirmation No. 8563
Title: METHODS AND APPARATUS FOR THE OPTIMIZATION OF PHOTO RESIST ETCHING IN A PLASMA PROCESSING SYSTEM	**CERTIFICATE OF MAILING** I hereby certify that this correspondence is being deposited with the US Postal Service as First Class Mail in a postage-paid envelope addressed to the Commissioner for Patents, P.O Box 1450, Alexandria, VA 22313-1450 on March 3, 2005. Signed: /Hanh H. Bui/ Hanh H. Bui

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449 may be material to the patentability of the above-identified patent application. Applicants submit the list of these references in compliance with their duty of disclosure pursuant to 37 CFR §§ 1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is believed to be filed after the mailing date of a first Office Action on the merits. A credit card payment of $180.00 is enclosed. However, if it is determined that additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 50-2284 (Order No. LMRX-P029).

Respectfully submitted,
By: __/Joseph Nguyen/____
Joseph Nguyen
Reg. No. 37,899

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US PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Publication Date	Name of Patentee or Applicant	Reference to Related Case
	1	6,083,844	2000-07-04	Bui-Le et al.	
	2	6,297163	2001-10-02	Zhu et al.	
	3	6,235,644 B1	2001-05-22	Chou	

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	5	"Research", http://graves-lab.cchem.berkeley.edu/~humbird/research/	
	6	Lassig et al., "Selective Removal Strategies for Low k Dual Damascene ", Semiconductor Fabtech, pp 185-190	
	7	EEE435/591 Microelectronics: Lecture 16: Back-end Processes	
	8	EE 539TM/M(S)E 599TM – Lecture C2: Lithography-based Systems	
	9	Hanawa, Tesuro (Group 1), "Current Status of Photolithography/Etching", Semiconductor Leading Edge Technologies, Inc. May 31, 2000 Selete Program Update	
	10	Jones et al., "Micro Photocell Monitoring Finds the Killers", Summer 2003, Yield Management Solutions, pp. 38-45	
	11	Woods, Eric, "Plasma Etching", CMOS Group, Microelectronics Research Center, Georgia Institute of Technology	
	12	Muscat, Anthony, "Gas Phase Cleaning of Silicon Wafer Surfaces", http://www.che.arizona.edu/directory/faculty/muscat/research/Tutorials/Gas_Phase_Wafer_Clean.html	
	13	Spitzlsperger, Gerhard, "Introduction to Low Pressure Glow Discharges for Semiconductor Manufacturing with Special Emphasis on Plasma Etching", http://www.gs68.de/tutorials/plasma/node26.html	

Examiner Signature		Date Considered	